WHAT IS CLAIMED IS:

1. A method of operating a memory cell that comprises a first junction region, a second junction region, a base, a nonconducting charge trapping layer and a gate, the method comprising:

performing a processing sequence including:

applying a voltage bias between the base and the gate to cause electrons to migrate towards and be retained in the trapping layer;

evaluating a read current generated in response to the voltage bias to determine whether a level of gate threshold voltage is reached; and

repeating the processing sequence a number of times by varying one or more time the voltage bias between the base and the gate until the level of gate threshold voltage is reached and the memory cell is in an erase state.

2. The method of claim 1, wherein applying a voltage bias between the base and the gate comprises applying a positive voltage to the gate and a negative voltage to the base.

3. The method of claim 1, wherein applying a voltage bias between the base and the gate comprises applying a positive voltage to the base and a negative voltage to the gate.

4. The method of claim 1, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the base and the gate comprises repeating the processing sequence by applying voltage pulses of unequal magnitudes to the base.

5. The method of claim 4, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the base and the gate further comprises repeating the processing sequence by applying voltage pulses of a constant magnitude to the gate.

6. The method of claim 1, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the base and the gate comprises repeating the processing sequence by applying ramped voltage pulses to the base.

7. The method of claim 6, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the base and the gate further comprises repeating the processing sequence by applying voltage pulses of a constant magnitude to the gate.

8. The method of claim 1, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the base and the gate

comprises repeating the processing sequence by applying voltage pulses of unequal magnitudes to the gate.

9. The method of claim 8, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the base and the gate further comprises repeating the processing sequence by applying voltage pulses of a constant magnitude to the base.

10. The method of claim 1, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the base and the gate comprises repeating the processing sequence by applying ramped voltage pulses to the gate.

11. The method of claim 10, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the base and the gate further comprises repeating the processing sequence by applying voltage pulses of a constant magnitude to the base.

12. The method of claim 1, wherein evaluating a read current generated in response to the voltage bias comprises

applying positive voltages respectively to the gate and one of the first or second junction region while grounding the other of the first or second junction region, thereby creating the read current; and

comparing the generated current with a predetermined current value.

13. A method of operating a memory cell that comprises a first junction region, a second junction region, a base, a nonconducting charge trapping layer and a gate, the method comprising:

setting the memory cell to an initial state of a first gate threshold voltage;

performing a processing sequence including:

applying a voltage bias between the gate and the first junction region to cause electric hole to migrate towards and be retained in the trapping layer;

evaluating a read current generated in response to the voltage bias to determine whether a second gate threshold voltage is reached, wherein the second gate threshold voltage is lower than the first gate threshold voltage; and

repeating the processing sequence a number of time by varying one or more time the voltage bias between the gate and the first junction region until the second gate threshold voltage is reached and the memory cell is in a program state.

14. The method of claim 13, wherein applying a voltage bias between the gate and the first junction region comprises applying a positive voltage to the first junction region and a negative voltage to the gate.

15. The method of claim 13, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the gate and the first junction region comprises repeating the processing sequence by applying voltage pulses of unequal magnitudes to the gate.

16. The method of claim 15, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the gate and the first junction region further comprises repeating the processing sequence by applying voltage pulses of a constant magnitude to the first junction.

17. The method of claim 13, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the gate and the first junction region comprises repeating the processing sequence by applying ramped voltage pulses to the gate.

18. The method of claim 17, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the gate and the first junction region further comprises repeating the processing sequence by applying voltage pulses of a constant magnitude to the first junction.

19. The method of claim 13, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the gate and the

first junction region comprises repeating the processing sequence by applying voltage pulses of unequal magnitudes to the first junction region.

20. The method of claim 19, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the gate and the first junction region further comprises repeating the processing sequence by applying voltage pulses of a constant magnitude to the gate.

21. The method of claim 13, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the gate and the first junction region comprises repeating the processing sequence by applying ramped voltage pulses to the first junction.

22. The method of claim 21, wherein repeating the processing sequence a number of times by varying one or more time the voltage bias between the gate and the first junction region further comprises repeating the processing sequence by applying voltage pulses of a constant magnitude to the gate.